501.39812VV2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YAMAZAKI, et al.

Application No.: TBD

Filed: August 13, 2003

For: FABRICATION METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Expected Group: 2822

Expected Examiner: S. Meier

CLAIM FOR PRIORITY

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 13, 2003

Sir:

Pursuant to 35 USC § 119 and 37 CFR §1.55, Applicants hereby claim priority based on prior Japanese Patent Application No. 2000-094986, filed in Japan on March 30, 2000.

The certified copy of the above-identified Japanese patent application was filed in Application No. 09/810,577, filed March 19, 2001, on June 26, 2001.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

William I. Solomon
Registration No. 28,565

WIS/sjg